UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/731,730	12/09/2003	Maneesh Soni	3226.1024-001	5151

21005 7590 09/20/2007

HAMILTON, BROOK, SMITH & REYNOLDS, P.C.
530 VIRGINIA ROAD
P.O. BOX 9133
CONCORD, MA 01742-9133

EXAMINER	
FLORES, LEON	

ART UNIT	PAPER NUMBER
2611	

MAIL DATE	DELIVERY MODE
09/20/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/731,730	SONI ET AL.	
	Examiner	Art Unit	
	Leon Flores	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 July 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 May 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments with respect to claims (1-14) have been considered but are moot in view of the new ground(s) of rejection.

Response to Remarks

Applicant asserts that, "Alexander does not pertain to processing of data samples, as in amended claim I, but to the analog processing of clock signals. Alexander does not disclose a tapped delay line able of storing samples, but a delay line made of delay elements that are buffers or inverters, which can only conduct and possible transform (e.g. invert) analog signals. Therefore Applicant contends that Alexander is a reference from a non-analogous art and that in cannot be used in an obviousness rejection".

The examiner respectfully disagrees. One skilled in the art would know that buffers are devices that can store data. Furthermore, the reference of Alexander is analogous to the present invention in the sense that it adjusts the length of a delay line in response to the output of a comparison between two signals.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

4. Claims (1-20) are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant admitted prior art (hereinafter "Prior art") in view of Alexander. (US Patent 6,765,419 B2)

Re claim 1, Prior art discloses a method of digitally processing samples comprising: reading the samples into a tapped delay chain (See Background of invention, page 2 lines 6-11); processing samples from taps on the delay chain (See Background of invention, page 2 lines 6-11).

But Prior art fails to teach that in response to receiving a signal of completion of a processing event, reducing the length of the delay chain by shifting samples rapidly out of the delay chain at a higher output rate than an input rate of samples coming into the delay chain.

However, Alexander does. (See figs 1-3 & col. 2, lines 15-22, col. 4, lines 16-25) Alexander discloses a method of reducing the length of a delay line in response to a control signal.

Therefore, taking the combined teachings of Prior art and Alexander as a whole. It would have been obvious to one of ordinary skills in the art to have incorporated this

feature into the system of Prior art, in the manner as claimed and as taught by Alexander, for the benefit of reducing the length of the delay chain.

Re claim 2, the combination of Prior art and Alexander further discloses that wherein the samples are from a data packet.

Re claim 3, the combination of Prior art and Alexander further discloses that wherein the data packet conforms to transmission system selected from the group of 802.11a, 802.11g and HIPERLAN/2 transmission systems. (In Prior art, see Background of invention, page 2 lines 6-11)

Re claim 4, the combination of Prior art and Alexander further discloses that wherein the event includes a synchronization of the data packet. (In Prior art, see Background of invention, page 2 lines 6-11)

Re claim 5, the combination of Prior art and Alexander further discloses that wherein the delay chain comprises a plurality of pipelined registers. (In Alexander, see col. 3, lines 49-50)

Re claim 6, the combination of Prior art and Alexander further discloses that wherein the reducing the length of the delay chain is performed until a desired length of the delay chain is achieved. (See col. 2, lines 15-22)

Re claim 7, the combination of Prior art and Alexander further discloses that wherein reducing the length of the delay chain further includes bypassing empty registers. (In Alexander, see fig. 3 & col. 5, lines 10-11, lines 40-44)

Re claim 8, Prior art discloses a method of digitally processing samples of a data packet comprising: reading the samples from a data packet into a tapped delay chain comprising a plurality of pipelined registers (See Background of invention, page 2 lines 6-11); processing samples from taps on the delay chain to synchronize a data packet (See Background of invention, page 2 lines 6-11);

But Prior art fails to teach that in response to receiving a signal of completion of a processing event, reducing the length of the delay chain by shifting samples rapidly out of the delay chain at a higher output rate than an input rate of samples coming into the delay chain by bypassing empty registers; and repeating the steps of reducing the length of the delay chain.

However, Alexander does. (See figs 1-3 & col. 2, lines 15-22, col. 4, lines 16-25) Alexander discloses a method of reducing the length of a delay line in response to a control signal.

Therefore, taking the combined teachings of Prior art and Alexander as a whole. It would have been obvious to one of ordinary skills in the art to have incorporated this feature into the system of Prior art, in the manner as claimed and as taught by Alexander, for the benefit of reducing the length of the delay chain.

Claim 9 is system claim corresponding to method claim 1. Hence, the steps performed in method claim 1 would have necessitated the elements in system claim 9. Therefore, claim 9 has been analyzed and rejected w/r to claim 1 above.

Claim 10 is system claim corresponding to method claim 2. Hence, the steps performed in method claim 2 would have necessitated the elements in system claim 10. Therefore, claim 10 has been analyzed and rejected w/r to claim 2 above.

Claim 11 is system claim corresponding to method claim 3. Hence, the steps performed in method claim 3 would have necessitated the elements in system claim 11. Therefore, claim 11 has been analyzed and rejected w/r to claim 3 above.

Re claim 12, the combination of Prior art and Alexander further discloses a timing recovery module for synchronization of the data packet that initiates a transition in the processor. (In Prior art, see Background of invention, page 2 lines 6-11)

Claim 13 is system claim corresponding to method claim 1. Hence, the steps performed in method claim 1 would have necessitated the elements in system claim 13. Therefore, claim 13 has been analyzed and rejected w/r to claim 1 above.

Claim 14 is system claim corresponding to method claim 1. Hence, the steps performed in method claim 1 would have necessitated the elements in system claim 14. Therefore, claim 14 has been analyzed and rejected w/r to claim 1 above.

Claim 15 has been analyzed and rejected w/r to claim 1 above.

Re claim 16, the combination of Prior art and Alexander further discloses bypassing an empty portion of delay chain. (In Alexander, see fig. 3 & col. 5, lines 10-11, lines 40-44)

Re claim 17, the combination of Prior art and Alexander further discloses that performed in response to receiving a signal of completion of a processing event. (In Alexander, see figs 1-3 & col. 2, lines 15-22, col. 4, lines 16-25)

Re claim 18, the combination of Prior art and Alexander further discloses that wherein the data samples are from a data packet signal of completion of a processing event is a sync signal indicating synchronization of the data packet. (In Prior art, see Background of invention, page 2 lines 6-11)

Re claim 19, the combination of Prior art and Alexander further discloses that wherein the processor is a state-machine. (In Prior art, see Background of invention,

page 2 lines 6-11. One skilled in the art would know that the processor can be a state-machine.)

Re claim 20, the combination of Prior art and Alexander further discloses that wherein the processor is a state-machine. (In Prior art, see Background of invention, page 2 lines 6-11. One skilled in the art would know that the processor can be a state-machine.)

Conclusion

5. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Contact

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Leon Flores whose telephone number is 571-270-1201. The examiner can normally be reached on Mon-Fri 7-5pm Alternate Fridays off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Payne can be reached on 571-272-3024. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

LF
September 7, 2007

DAVID C. PAYNE
SUPERVISORY PATENT EXAMINER